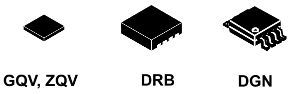


1.25-W MONO FULLY DIFFERENTIAL AUDIO POWER AMPLIFIER

FEATURES

- **1.25 W Into 8 Ω From a 5-V Supply at THD = 1% (Typical)**
- **Low Supply Current: 1.7 mA Typical**
- **Shutdown Control < 10 μA**
- **Only Five External Components**
  - **Improved PSRR (90 dB) and Wide Supply Voltage (2.5 V to 5.5 V) for Direct Battery Operation**
  - **Fully Differential Design Reduces RF Rectification**
  - **Improved CMRR Eliminates Two Input Coupling Capacitors**
  - **$C_{(BYPASS)}$ Is Optional Due to Fully Differential Design and High PSRR**
- **Avaliable in a 2 mm x 2 mm MicroStar Junior ™ BGA Package (GQV, ZQV)**
- **Available in 3 mm x 3 mm QFN Package (DRB)**
- **Available in an 8-Pin PowerPAD™ MSOP (DGN)**

APPLICATIONS

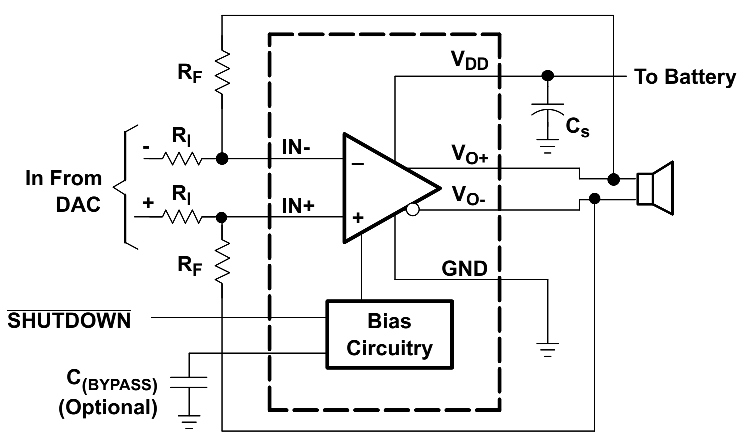
- **Designed for Wireless or Cellular Handsets and PDAs**

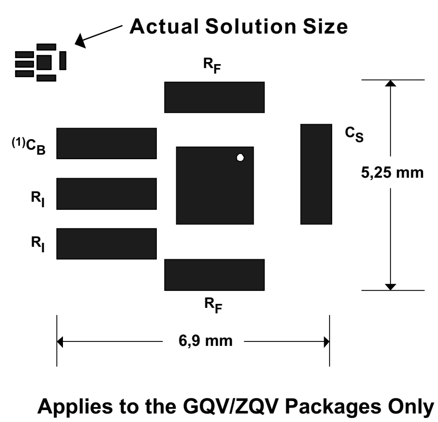
DESCRIPTION

The TPA6203A1 is a 1.25-W mono fully differential amplifier designed to drive a speaker with at least 8-Ω impedance while consuming less than 37 mm^2 (ZQV package option) total printed-circuit board (PCB) area in most applications. This device operates from 2.5 V to 5.5 V, drawing only 1.7 mA of quiescent supply current. The TPA6203A1 is available in the space-saving 2 mm x 2 mm MicroStar Junior™ BGA package, and the space saving 3 mm x 3 mm QFN (DRB) package.

Features like 85-dB PSRR from 90 Hz to 5 kHz, improved RF-rectification immunity, and small PCB area makes the TPA6203A1 ideal for wireless handsets. A fast start-up time of 4 μs with minimal pop makes the TPA6203A1 ideal for PDA applications.

APPLICATION CIRCUIT





Applies to the GQV/ZQV Packages Only

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

	PACKAGED DEVICES (1) (2) (3)			
	MicroStar Junior™ (GQV)	MicroStar Junior™ (ZQV)	QFN (DRB)	MSOP (DGN)
Device	TPA6203A1GQVR	TPA6203A1ZQVR	TPA6203A1DRB	TPA6203A1DGN
Symbolization	AADI	AAEI	AAJI	AAII

(1) The GQV is the standard MicroStar Junior package. The ZQV is a lead-free option and is qualified for 260° lead-free assembly.
(2) The GQV and ZQV packages are only available taped and reeled. The suffix R designates taped and reeled parts.
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

			UNIT
Supply voltage, V_{DD}			-0.3 V to 6 V
Input voltage, V_I	INx and $\overline{\text{SHUTDOWN}}$ pins		-0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation			See Dissipation Rating Table
Operating free-air temperature, T_A			-40°C to 85°C
Junction temperature, T_J			-40°C to 125°C
Storage temperature, T_{stg}			-65°C to 85°C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds		ZQV, DRB, DGN	260°C
		GQV	235°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}		2.5		5.5	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$	2			V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$			0.8	V
Common-mode input voltage, V_{IC}	V_{DD} = 2.5 V, 5.5 V, CMRR ≤ -60 dB	0.5		V_{DD}-0.8	V
Operating free-air temperature, T_A		-40		85	°C
Load impedance, Z_L		6.4	8		Ω

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
GQV, ZQV	885 mW	8.8 mW/°C	486 mW	354 mW
DRB	2.7 W	21.8 mW/°C	1.7 W	1.4 W

ELECTRICAL CHARACTERISTICS

T_A = 25°C, Gain = 1 V/V

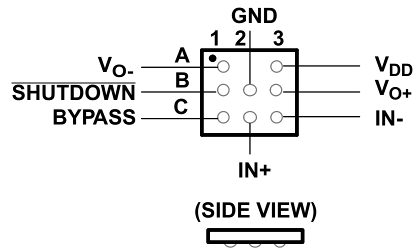
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_I = 0 V, V_{DD} = 2.5 V to 5.5 V				9	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V			-90	-70	dB
CMRR	Common-mode rejection ratio	V_{DD} = 3.6 V to 5.5 V, V_{IC} = 0.5 V to V_{DD}-0.8			-70	-65	dB
		V_{DD} = 2.5 V, V_{IC} = 0.5 V to 1.7 V			-62	-55	
V_{OL}	Low-level output voltage	R_L = 8 Ω, V_{IN+} = V_{DD}, V_{IN-} = 0 V or V_{IN+} = 0 V, V_{IN-} = V_{DD}	V_{DD} = 5.5 V		0.30	0.46	V
			V_{DD} = 3.6 V		0.22		
			V_{DD} = 2.5 V		0.19	0.26	
V_{OH}	High-level output voltage	R_L = 8 Ω, V_{IN+} = V_{DD}, V_{IN-} = 0 V or V_{IN+} = 0 V, V_{IN-} = V_{DD}	V_{DD} = 5.5 V	4.8	5.12		V
			V_{DD} = 3.6 V		3.28		
			V_{DD} = 2.5 V	2.1	2.24		
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = 5.8 V				1.2	μA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = -0.3 V				1.2	μA
I_{DD}	Supply current	V_{DD} = 2.5 V to 5.5 V, No load, $\overline{SHUTDOWN}$ = 2 V			1.7	2	mA
$I_{DD(SD)}$	Supply current in shutdown mode	$\overline{SHUTDOWN}$ = 0.8 V, V_{DD} = 2.5 V to 5.5 V, No load			0.01	0.9	μA

OPERATING CHARACTERISTICS

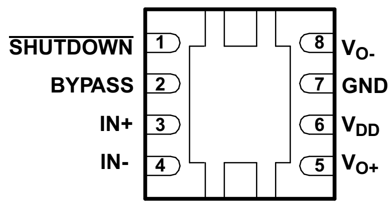
T_A = 25°C, Gain = 1 V/V, R_L = 8 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N = 1%, f = 1 kHz	V_{DD} = 5 V		1.25		W
			V_{DD} = 3.6 V		0.63		
			V_{DD} = 2.5 V		0.3		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5 V, P_O = 1 W, f = 1 kHz			0.06%		
		V_{DD} = 3.6 V, P_O = 0.5 W, f = 1 kHz			0.07%		
		V_{DD} = 2.5 V, P_O = 200 mW, f = 1 kHz			0.08%		
k_{SVR}	Supply ripple rejection ratio	$C_{(BYPASS)}$ = 0.47 °F, V_{DD} = 3.6 V to 5.5 V, Inputs ac-grounded with C_I = 2 μF	f = 217 Hz to 2 kHz, V_{RIPPLE} = 200 mV_{PP}		-87		dB
		$C_{(BYPASS)}$ = 0.47 μF, V_{DD} = 2.5 V to 3.6 V, Inputs ac-grounded with C_I = 2 μF	f = 217 Hz to 2 kHz, V_{RIPPLE} = 200 mV_{PP}		-82		
		$C_{(BYPASS)}$ = 0.47 μF, V_{DD} = 2.5 V to 5.5 V, Inputs ac-grounded with C_I = 2 μF	f = 40 Hz to 20 kHz, V_{RIPPLE} = 200 mV_{PP}		≤-74		
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O= 1 W			104		dB
V_n	Output voltage noise	f = 20 Hz to 20 kHz	No weighting		17		μV_{RMS}
			A weighting		13		
CMRR	Common-mode rejection ratio	V_{DD} = 2.5 V to 5.5 V, resistor tolerance = 0.1%, gain = 4V/V, V_{ICM} = 200 mV_{PP}	f = 20 Hz to 1 kHz		≤-85		dB
			f = 20 Hz to 20 kHz		≤-74		
Z_I	Input impedance				2		MΩ
Z_O	Output impedance	Shutdown mode		>10k			
	Shutdown attenuation	f = 20 Hz to 20 kHz, R_F = R_I = 20 kΩ			-80		dB

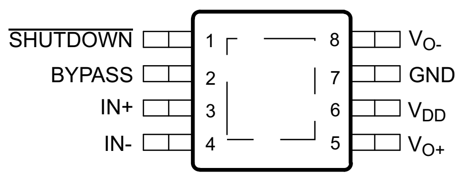
MicroStar Junior™ (GQV or ZQV) PACKAGE
(TOP VIEW)



8-PIN QFN (DRB) PACKAGE
(TOP VIEW)



8-PIN MSOP (DGN) PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	GQV	DRB, DGN		
BYPASS	C1	2	I	Mid-supply voltage. Adding a bypass capacitor improves PSRR.
GND	B2	7	I	High-current ground
IN-	C3	4	I	Negative differential input
IN+	C2	3	I	Positive differential input
SHUTDOWN	B1	1	I	Shutdown terminal (active low logic)
V_{DD}	A3	6	I	Supply voltage terminal
V_{O+}	B3	5	O	Positive BTL output
V_{O-}	A1	8	O	Negative BTL output
Thermal Pad				Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
P_O	Output power	vs Supply voltage	1
		vs Load resistance	2, 3
P_D	Power dissipation	vs Output power	4, 5
	Maximum ambient temperature	vs Power dissipation	6
	Total harmonic distortion + noise	vs Output power	7, 8
		vs Frequency	9, 10, 11, 12
		vs Common-mode input voltage	13
	Supply voltage rejection ratio	vs Frequency	14, 15, 16, 17
	Supply voltage rejection ratio	vs Common-mode input voltage	18
	GSM Power supply rejection	vs Time	19
	GSM Power supply rejection	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
		vs Common-mode input voltage	22
	Closed loop gain/phase	vs Frequency	23
	Open loop gain/phase	vs Frequency	24
I_{DD}	Supply current	vs Supply voltage	25
		vs Shutdown voltage	26
	Start-up time	vs Bypass capacitor	27

TYPICAL CHARACTERISTICS

OUTPUT POWER vs SUPPLY VOLTAGE

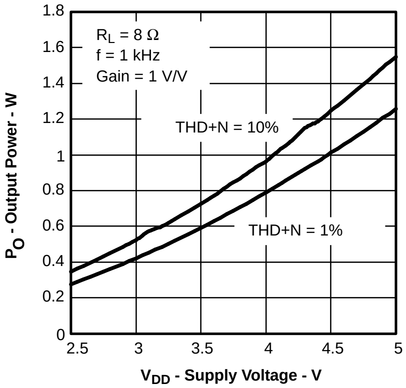


Figure 1.

OUTPUT POWER vs LOAD RESISTANCE

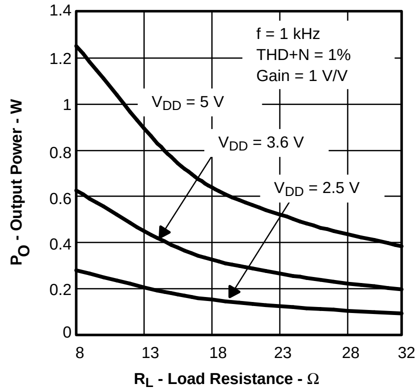


Figure 2.

OUTPUT POWER vs LOAD RESISTANCE

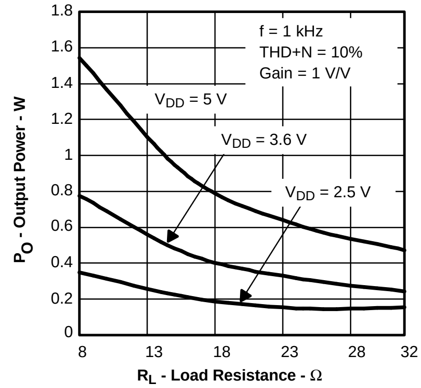


Figure 3.

POWER DISSIPATION vs OUTPUT POWER

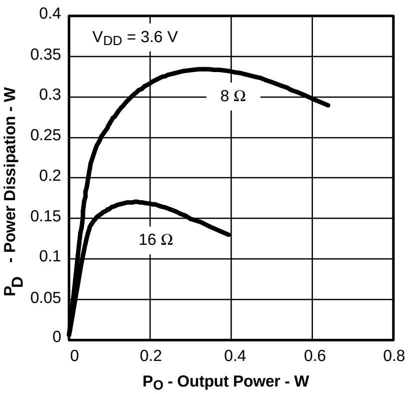


Figure 4.

POWER DISSIPATION vs OUTPUT POWER

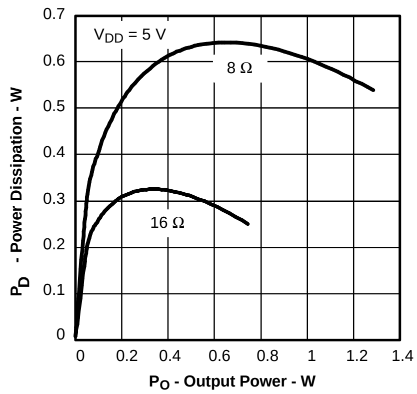


Figure 5.

MAXIMUM AMBIENT TEMPERATURE vs POWER DISSIPATION

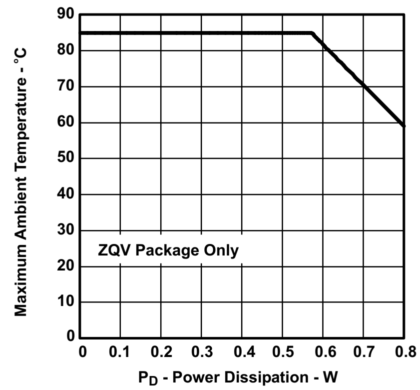


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

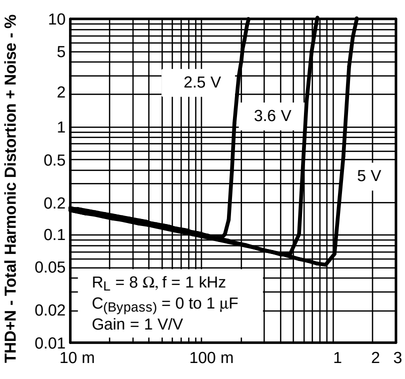


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

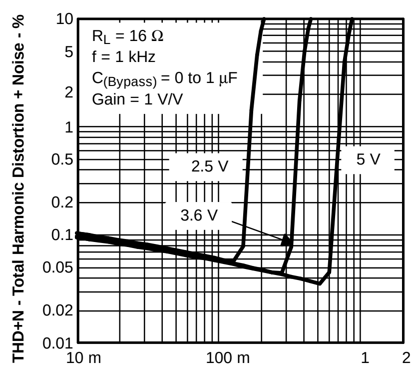


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

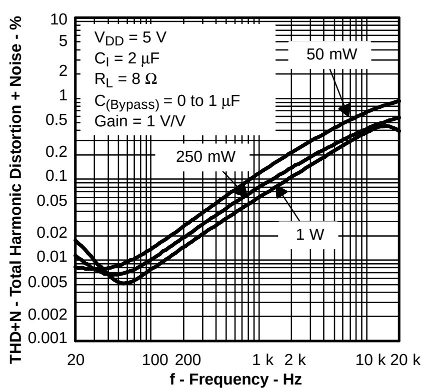


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

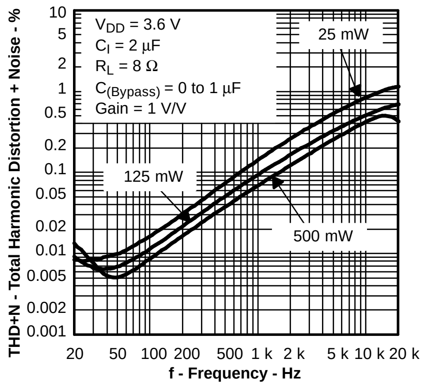


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

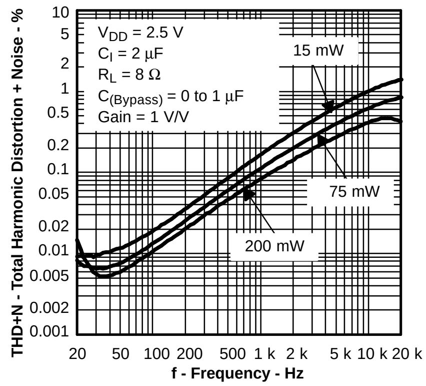


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

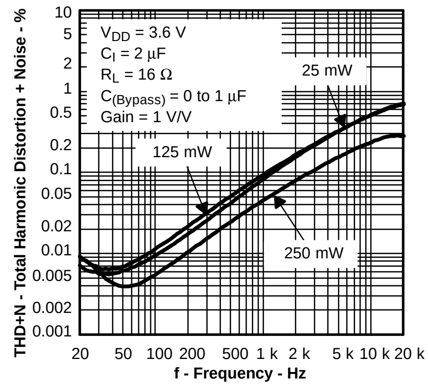


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs COMMON MODE INPUT VOLTAGE

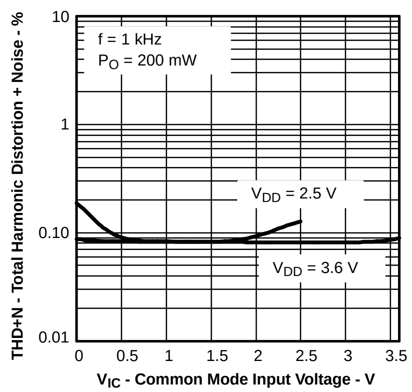


Figure 13.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

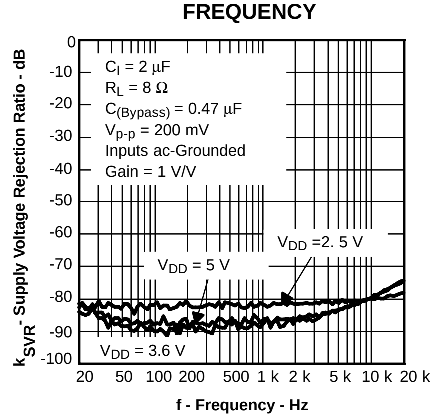


Figure 14.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

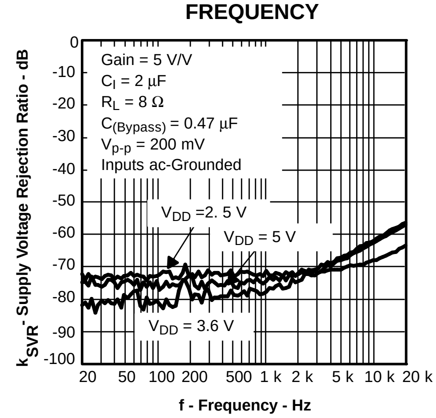


Figure 15.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

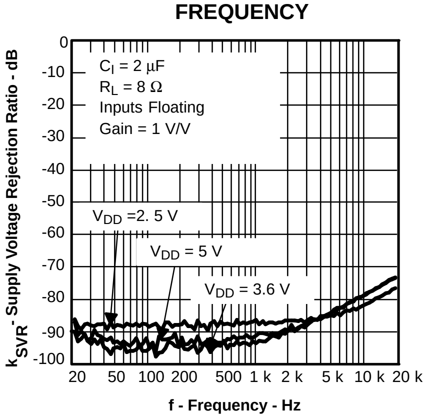


Figure 16.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

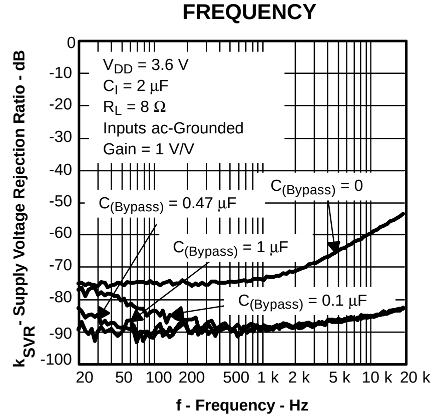


Figure 17.

SUPPLY VOLTAGE REJECTION RATIO vs COMMON MODE INPUT VOLTAGE

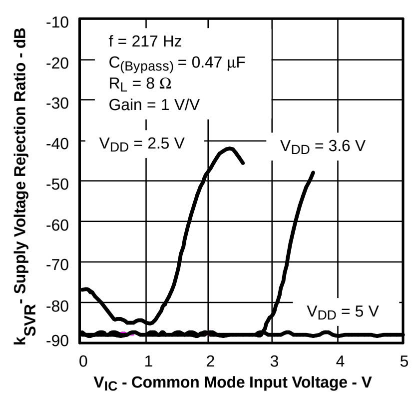


Figure 18.

TYPICAL CHARACTERISTICS (continued)

GSM POWER SUPPLY REJECTION vs TIME

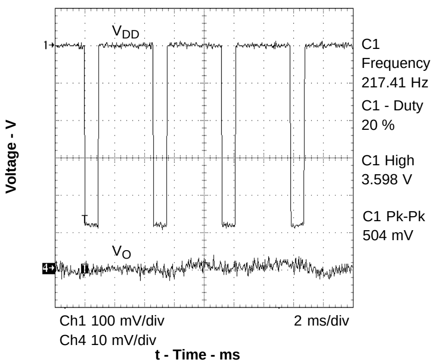


Figure 19.

GSM POWER SUPPLY REJECTION vs FREQUENCY

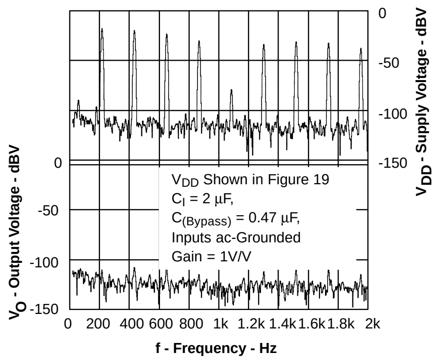


Figure 20.

COMMON MODE REJECTION RATIO vs FREQUENCY

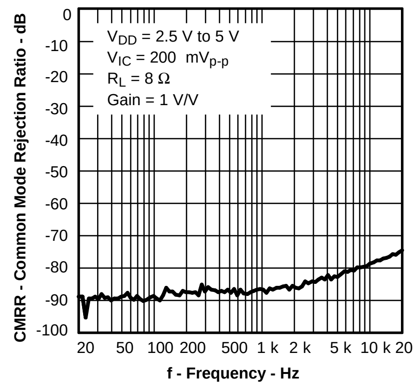


Figure 21.

COMMON MODE REJECTION RATIO vs COMMON MODE INPUT VOLTAGE

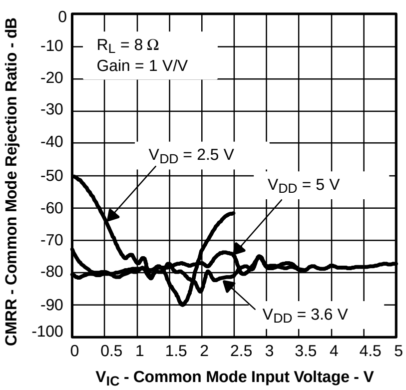


Figure 22.

CLOSED LOOP GAIN/PHASE vs FREQUENCY

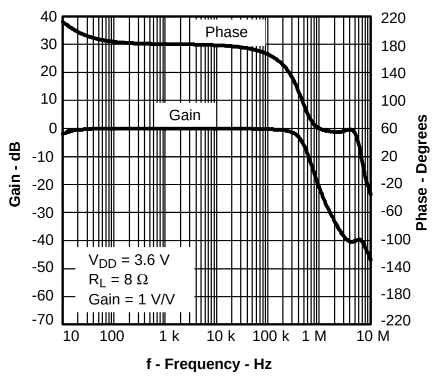


Figure 23.

OPEN LOOP GAIN/PHASE vs FREQUENCY

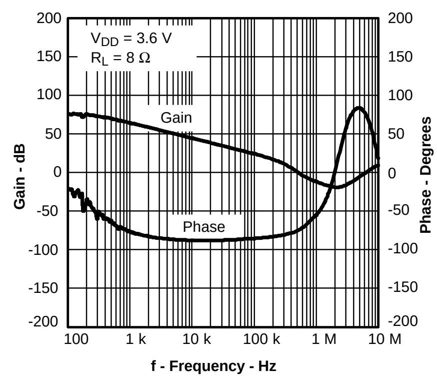


Figure 24.

SUPPLY CURRENT vs SUPPLY VOLTAGE

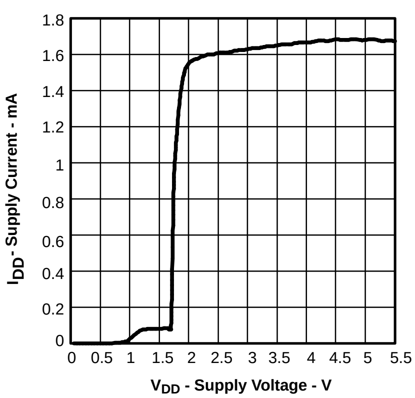


Figure 25.

SUPPLY CURRENT vs SHUTDOWN VOLTAGE

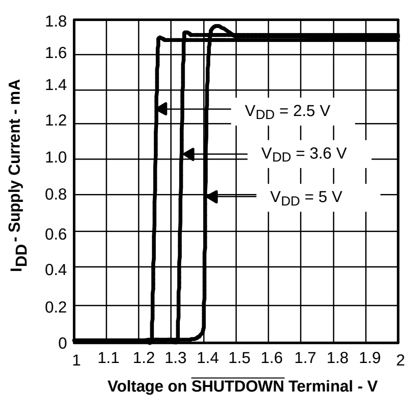
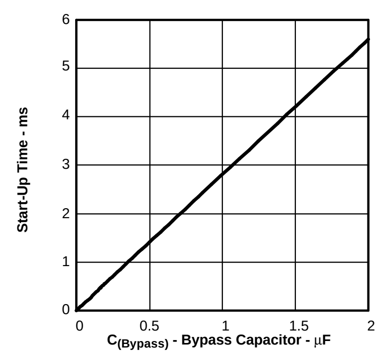


Figure 26.

START-UP TIME[(1)] vs BYPASS CAPACITOR



(1) Start-Up time is the time it takes (from a low-to-high transition on SHUTDOWN) for the gain of the amplifier to reach -3 dB of the final gain.

Figure 27.

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The TPA6203A1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common- mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common- mode voltage at the input.

Advantages of Fully Differential Amplifiers

- Input coupling capacitors not required: A fully differential amplifier with good CMRR, like the TPA6203A1, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has mid-supply lower than the mid-supply of the TPA6203A1, the common-mode feedback circuit adjusts for that, and the TPA6203A1 outputs are still biased at mid-supply of the TPA6203A1. The inputs of the TPA6203A1 can be biased from 0.5 V to V_{DD} - 0.8 V. If the inputs are biased outside of that range, input coupling capacitors are required.
- Mid-supply bypass capacitor, $C_{(BYPASS)}$, not required: The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output. However, removing the bypass capacitor slightly worsens power supply rejection ratio (k_{SVR}), but a slight decrease of k_{SVR} may be acceptable when an additional component can be eliminated (see Figure 17).
- Better RF-immunity: GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

APPLICATION SCHEMATICS

Figure 28 through Figure 30 show application schematics for differential and single-ended inputs. Typical values are shown in Table 1.

Table 1. Typical Component Values

COMPONENT	VALUE
R_I	10 kΩ
R_F	10 kΩ
$C_{(BYPASS)}$(1)	0.22 µF
C_S	1 µF
C_I	0.22 µF

(1) $C_{(BYPASS)}$ is optional

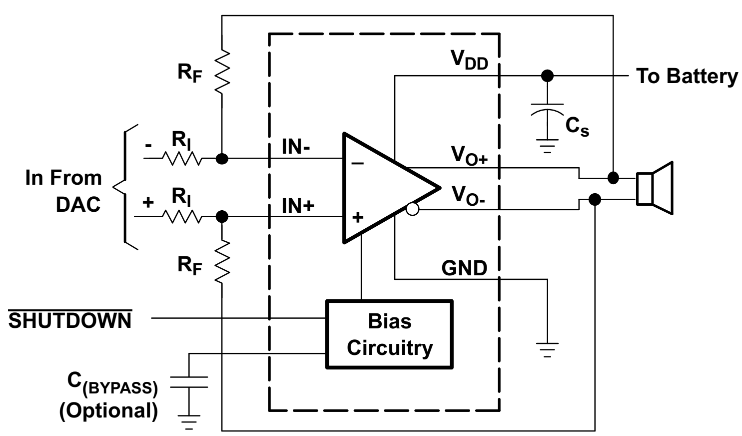


Figure 28. Typical Differential Input Application Schematic

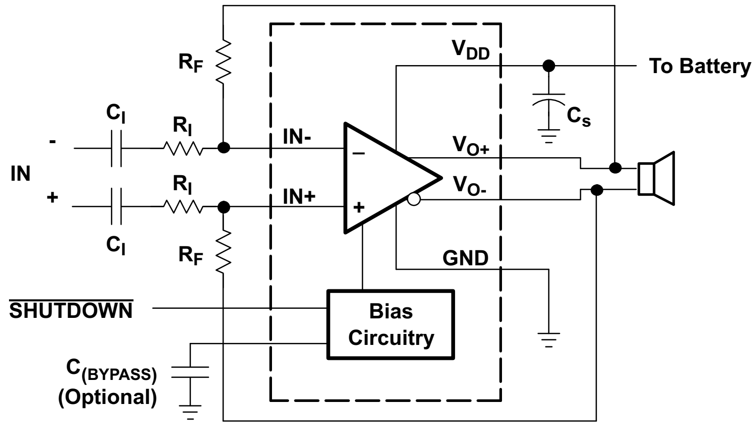


Figure 29. Differential Input Application Schematic Optimized With Input Capacitors

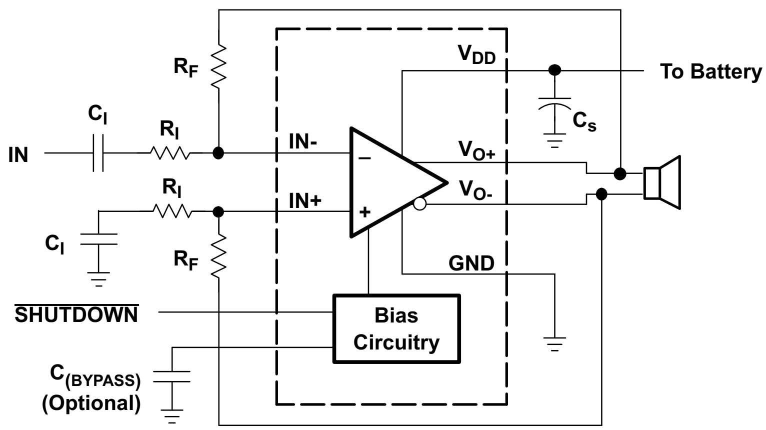


Figure 30. Single-Ended Input Application Schematic

Selecting Components

Resistors (R_F and R_I)

The input (R_I) and feedback resistors (R_F) set the gain of the amplifier according to Equation 1.

$$\text{Gain} = R_F/R_I \tag{1}$$

R_F and R_I should range from 1 kΩ to 100 kΩ. Most graphs were taken with $R_F = R_I = 20$ kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

Bypass Capacitor (C_{BYPASS}) and Start-Up Time

The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}/2$. Adding a capacitor to this pin filters any noise into this pin and increases the k_{SVR}. $C_{(BYPASS)}$also determines the rise time of V_{O+} and V_{O-} when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. Although the output rise time depends on the bypass capacitor value, the device passes audio 4 µs after taken out of shutdown and the gain is slowly ramped up based on $C_{(BYPASS)}$.

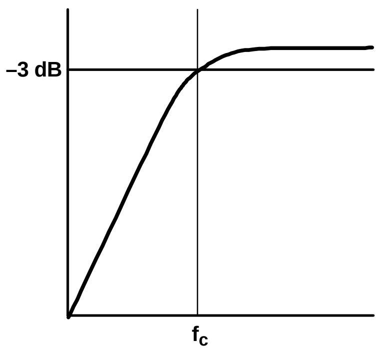
To minimize *pops* and *clicks*, design the circuit so the impedance (resistance and capacitance) detected by both inputs, IN+ and IN-, is equal.

Input Capacitor (C_I)

The TPA6203A1 does not require input coupling capacitors if using a differential input source that is biased from 0.5 V to V_{DD} - 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 2.

$$f_c = \frac{1}{2\pi R_I C_I} \qquad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 100 Hz. Equation 2 is reconfigured as Equation 3.

$$C_I = \frac{1}{2\pi R_I f_c} \qquad (3)$$

In this example, C_I is 0.16 µF, so one would likely choose a value in the range of 0.22 µF to 0.47 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_S)

The TPA6203A1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically 0.1 µF to 1 µF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

DIFFERENTIAL OUTPUT VERSUS SINGLE-ENDED OUTPUT

Figure 31 shows a Class-AB audio power amplifier (APA) in a fully differential configuration. The TPA6203A1 amplifier has differential outputs driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 4).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (4)$$

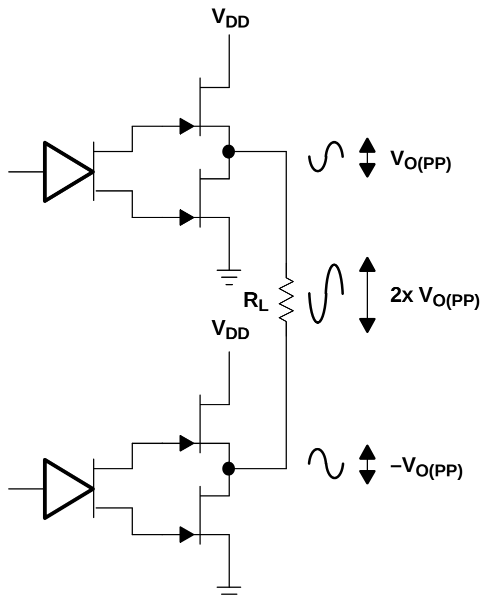


Figure 31. Differential Output Configuration

In a typical wireless handset operating at 3.6 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 200 mW to 800 mW. In sound power that is a 6-dB improvement—which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 32. A coupling capacitor is required to block the dc offset voltage from reaching the load. This capacitor can be quite large (approximately 33 µF to 1000 µF) so it tends to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency-limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 5.

$$f_C = \frac{1}{2\pi R_L C_C} \quad (5)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

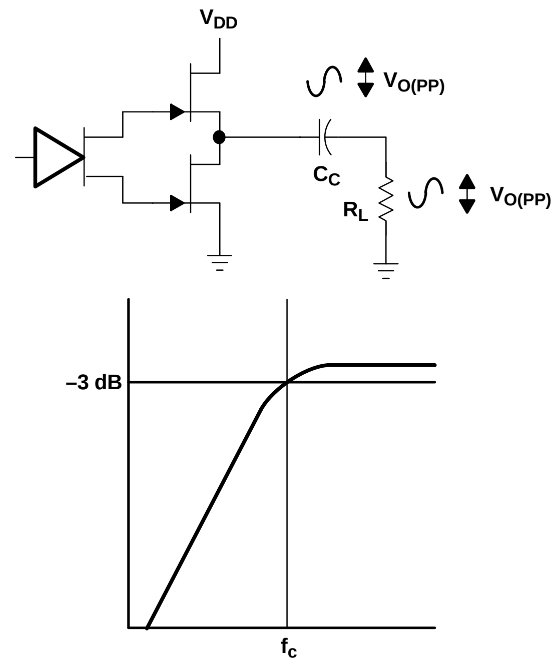


Figure 32. Single-Ended Output and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration.

FULLY DIFFERENTIAL AMPLIFIER EFFICIENCY AND THERMAL INFORMATION

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the average value of the supply current, I_{DD}(avg), determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 33).

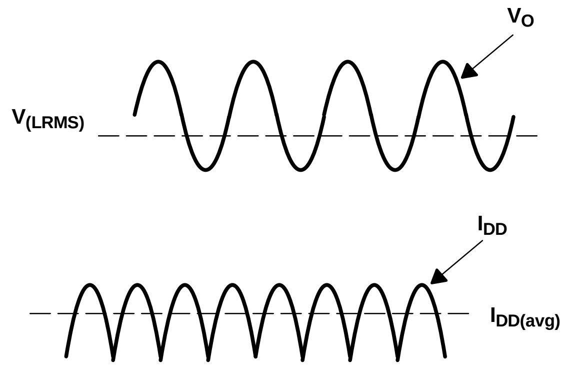


Figure 33. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\pi} \times \frac{V_P}{R_L}\,[\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\,V_{DD}\,V_P}{\pi\,R_L}$$

substituting P_L and P_{SUP} into equation 6,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\,R_L}}{\frac{2\,V_{DD}\,V_P}{\pi\,R_L}} = \frac{\pi\,V_P}{4\,V_{DD}}$$

where:

$$V_P = \sqrt{2\,P_L\,R_L}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
I_{DD}avg = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

(6)

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2 P_L R_L}}{4 V_{DD}} \quad (7)$$

Table 2. Efficiency and Maximum Ambient Temperature vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Internal Dissipation (W)	Power From Supply (W)	Max Ambient Temperature (°C)
0.25	31.4	0.55	0.75	62
0.50	44.4	0.62	1.12	54
1.00	62.8	0.59	1.59	58
1.25	70.2	0.53	1.78	65

Table 2 employs Equation 7 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 1.25-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 1.8 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in Equation 7, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

A simple formula for calculating the maximum power dissipated, P_{Dmax}, may be used for a differential output application:

$$P_{D\,max} = \frac{2 V_{DD}^2}{\pi^2 R_L} \quad (8)$$

P_{Dmax} for a 5-V, 8-Ω system is 634 mW.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the 2 mm x 2 mm Microstar Junior™ package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0088} = 113°C/W \quad (9)$$

Given θ_{JA}, the maximum allowable junction temperature, and the maximum internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA6203A1 is 125°C.

$$T_A\,Max = T_J\,Max - \Theta_{JA} P_{Dmax} = 125 - 113(0.634) = 53.3°C \quad (10)$$

Equation 10 shows that the maximum ambient temperature is 53.3°C at maximum power dissipation with a 5-V supply.

Table 2 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA6203A1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using more resistive than 8-Ω speakers dramatically increases the thermal performance by reducing the output current.

PCB LAYOUT

In making the pad size for the BGA balls, it is recommended that the layout use solder-mask-defined (SMD) land. With this method, the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique include more closely controlled size and better copper adhesion to the laminate. Increased copper also increases the thermal performance of the IC. Better size control is the result of photo imaging the stencils for masks. Small plated vias should be placed near the center ball connecting ball B2 to the ground plane. Added plated vias and ground plane act as a heatsink and increase the thermal performance of the device. Figure 34 shows the appropriate diameters for a 2 mm X 2 mm MicroStar Junior™ BGA layout.

It is very important to keep the TPA6203A1 external components very close to the TPA6203A1 to limit noise pickup. The TPA6203A1 evaluation module (EVM) layout is shown in the next section as a layout example.

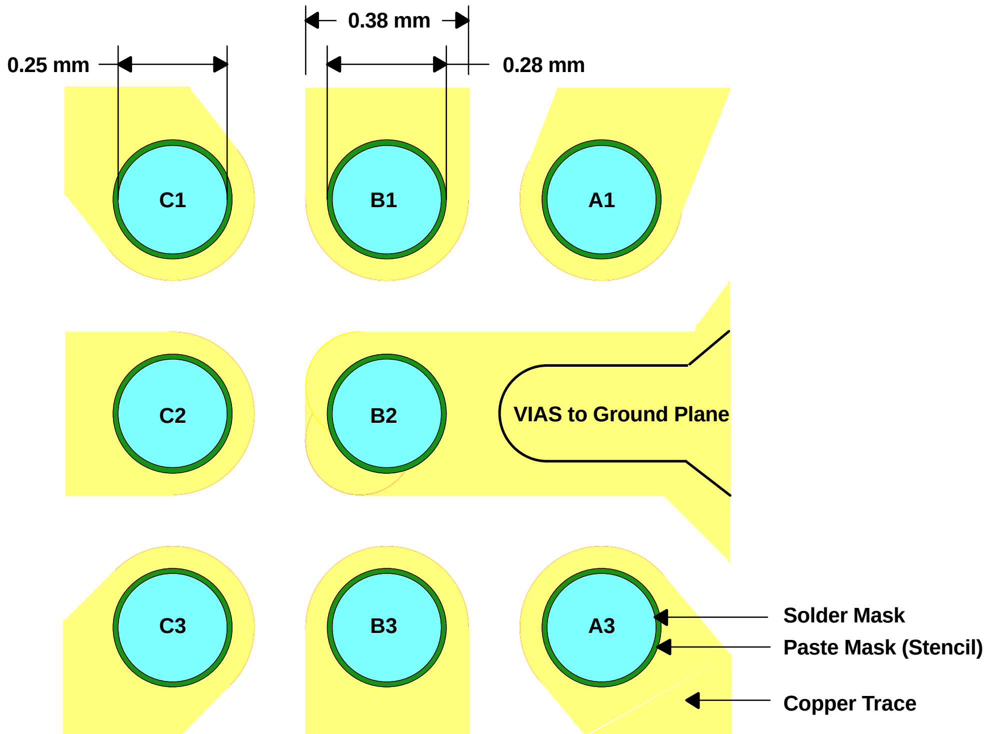


Figure 34. MicroStar Junior™ BGA Recommended Layout

8-Pin QFN (DRB) Layout

Use the following land pattern for board layout with the 8-pin QFN (DRB) package. Note that the solder paste should use a hatch pattern to fill solder paste at 50% to ensure that there is not too much solder paste under the package.

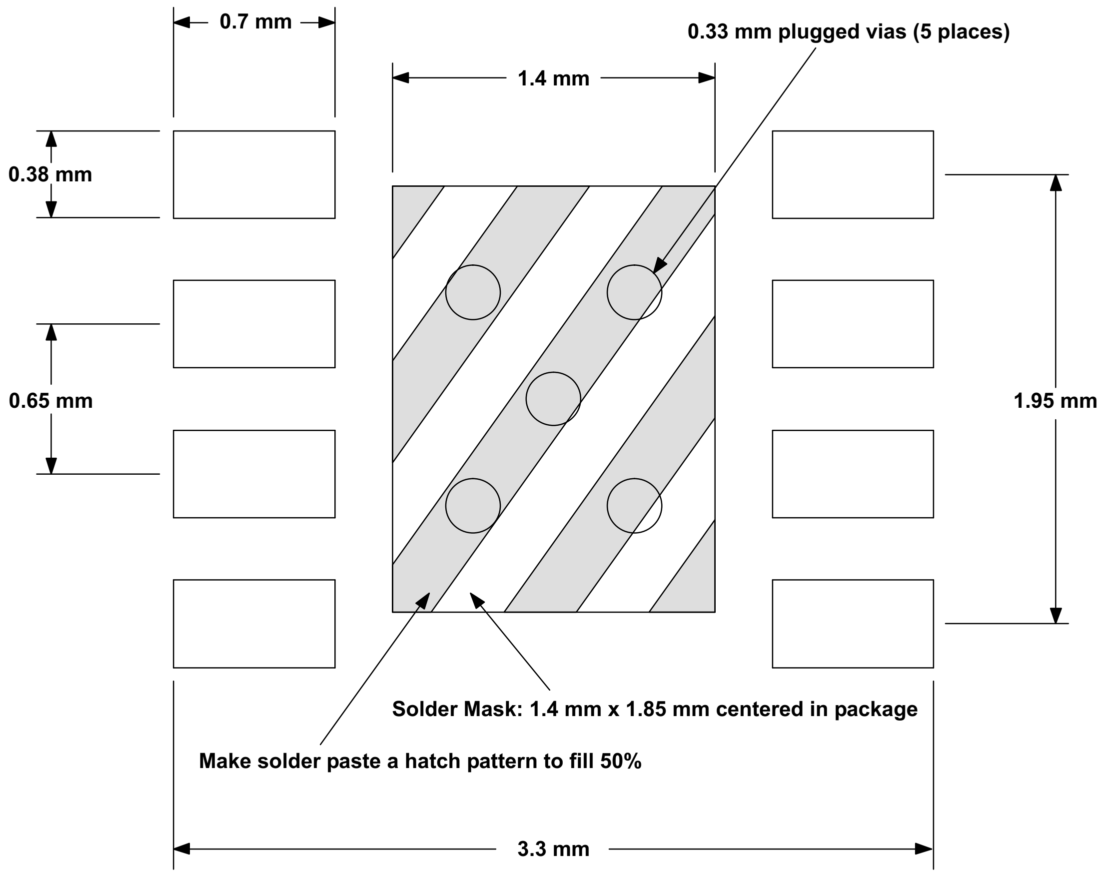


Figure 35. TPA6203A1 8-Pin QFN (DRB) Board Layout (Top View)

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPA6203A1DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6203A1DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6203A1DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6203A1DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6203A1DRB	ACTIVE	SON	DRB	8	121	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6203A1DRBG4	ACTIVE	SON	DRB	8	121	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6203A1DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6203A1DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6203A1GQVR	ACTIVE	BGA MI CROSTA R JUNI OR	GQV	8	2500	TBD	SNPB	Level-2A-235C-4 WKS
TPA6203A1ZQVR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQV	8	2500	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168HRS

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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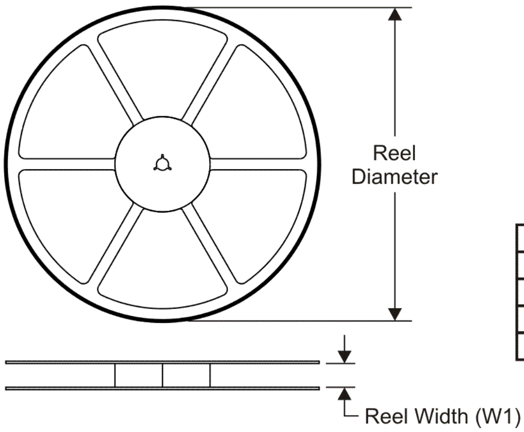
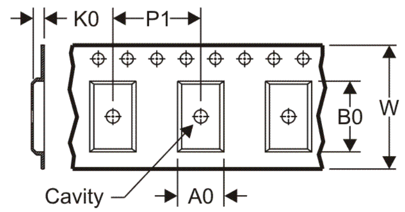
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

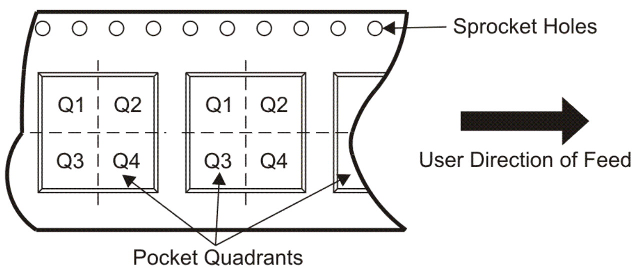


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

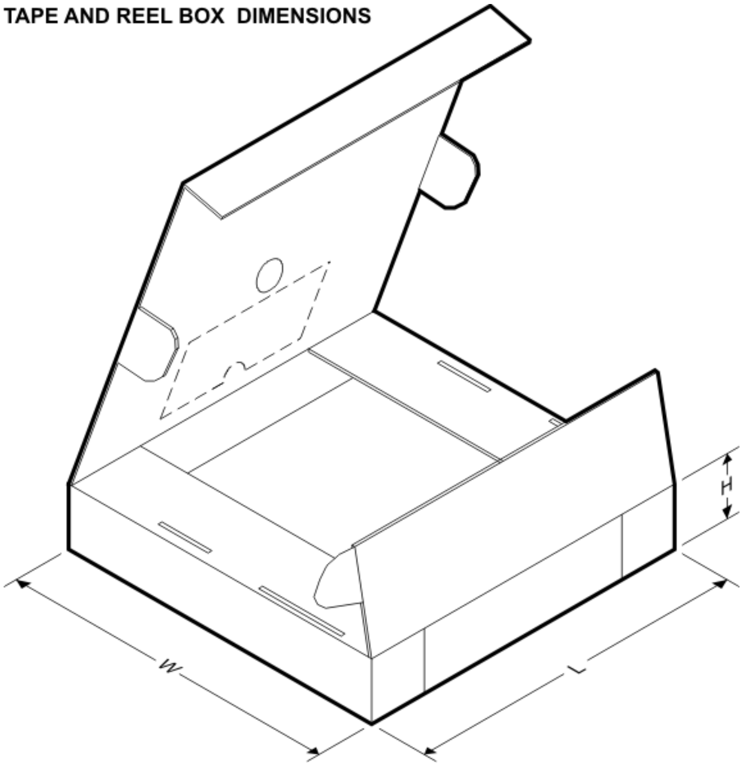
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6203A1DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6203A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6203A1GQVR	BGA MI CROSTA R JUNI OR	GQV	8	2500	330.0	8.4	2.3	2.3	1.4	4.0	8.0	Q1
TPA6203A1ZQVR	BGA MI CROSTA R JUNI OR	ZQV	8	2500	330.0	8.4	2.3	2.3	1.4	4.0	8.0	Q1

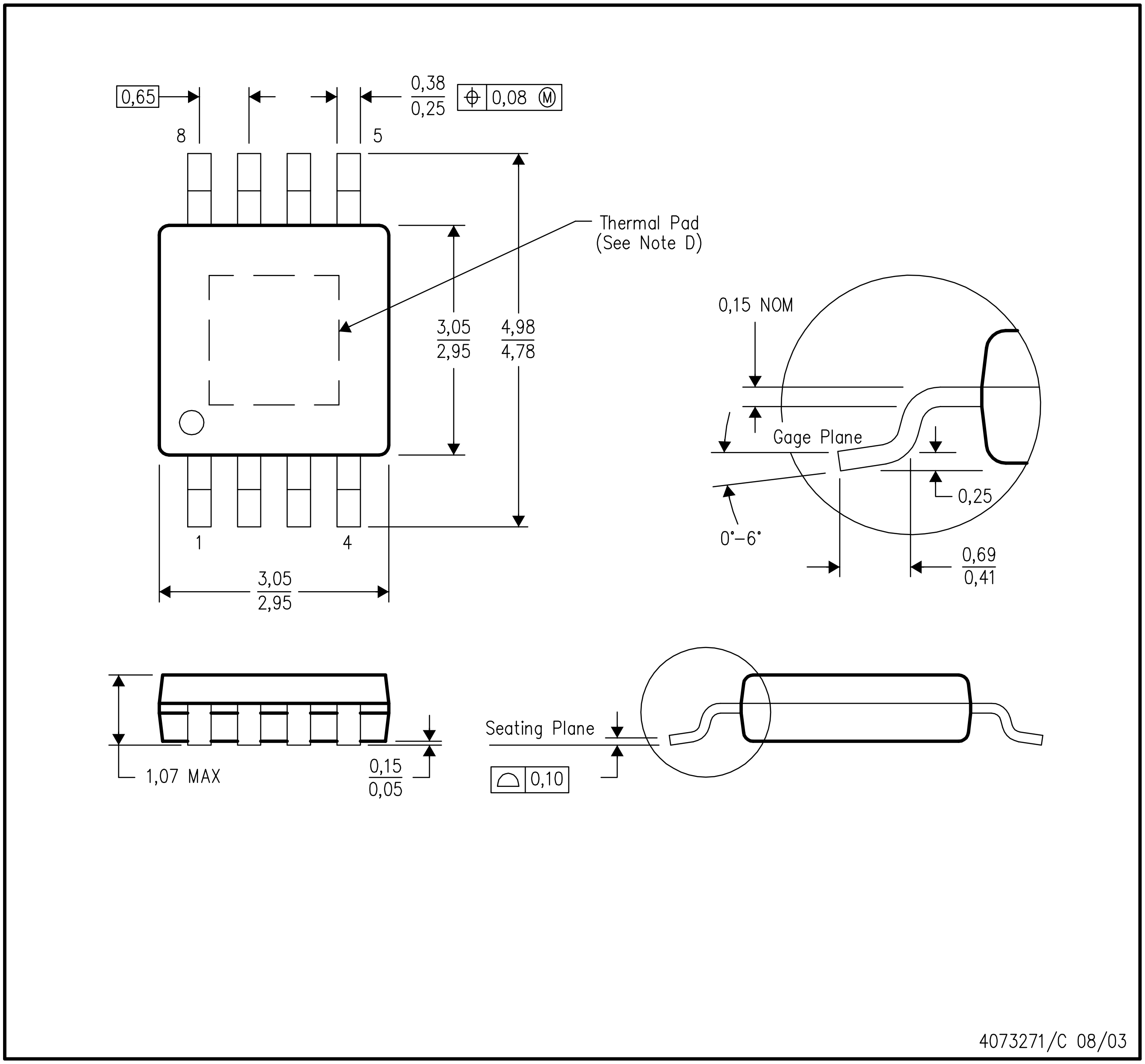
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6203A1DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	29.0
TPA6203A1DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPA6203A1GQVR	BGA MICROSTAR JUNIOR	GQV	8	2500	340.5	333.0	20.6
TPA6203A1ZQVR	BGA MICROSTAR JUNIOR	ZQV	8	2500	340.5	333.0	20.6

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



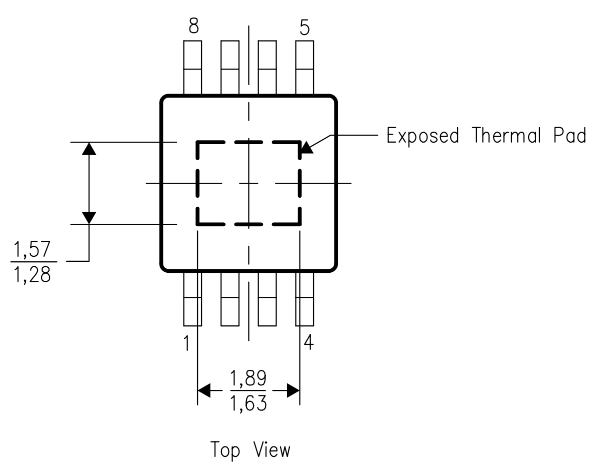
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO-187

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

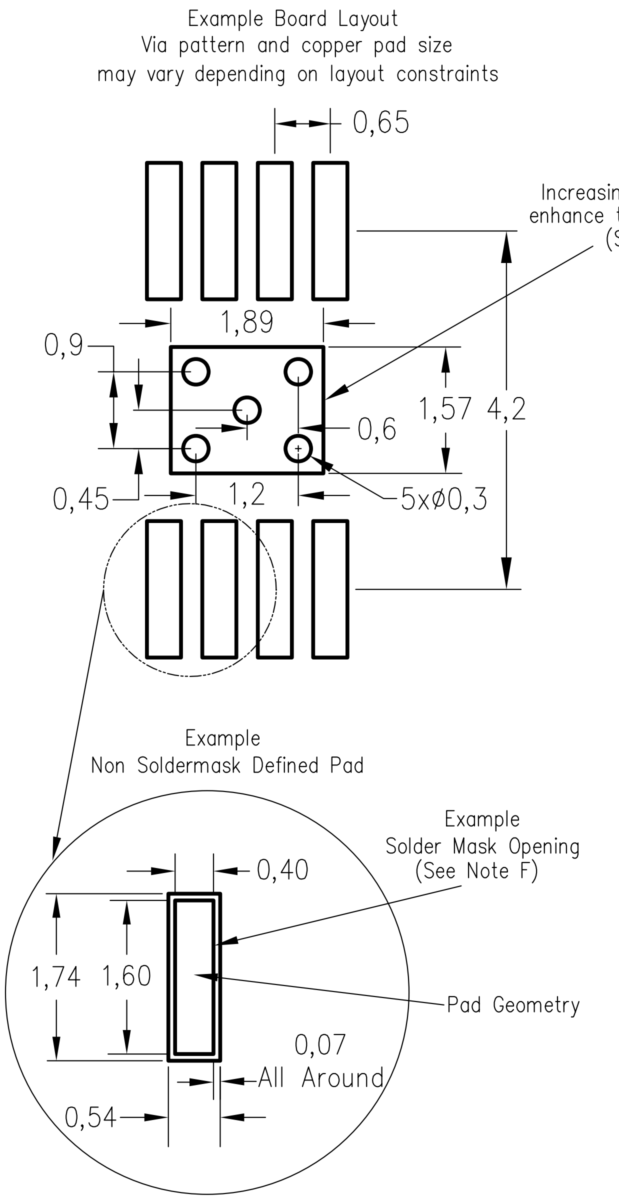
The exposed thermal pad dimensions for this package are shown in the following illustration.

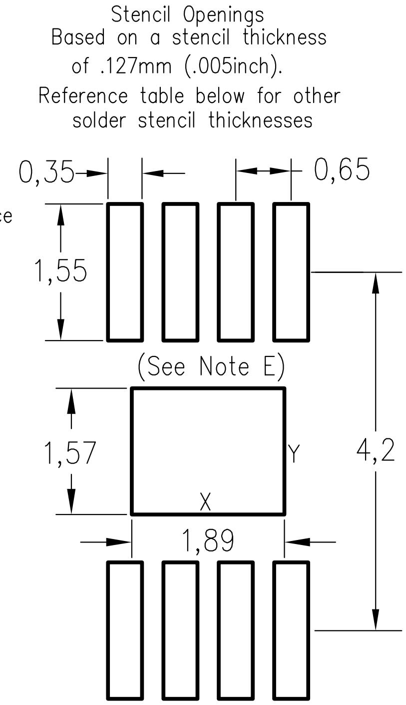


NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R-PDSO-G8) PowerPAD™





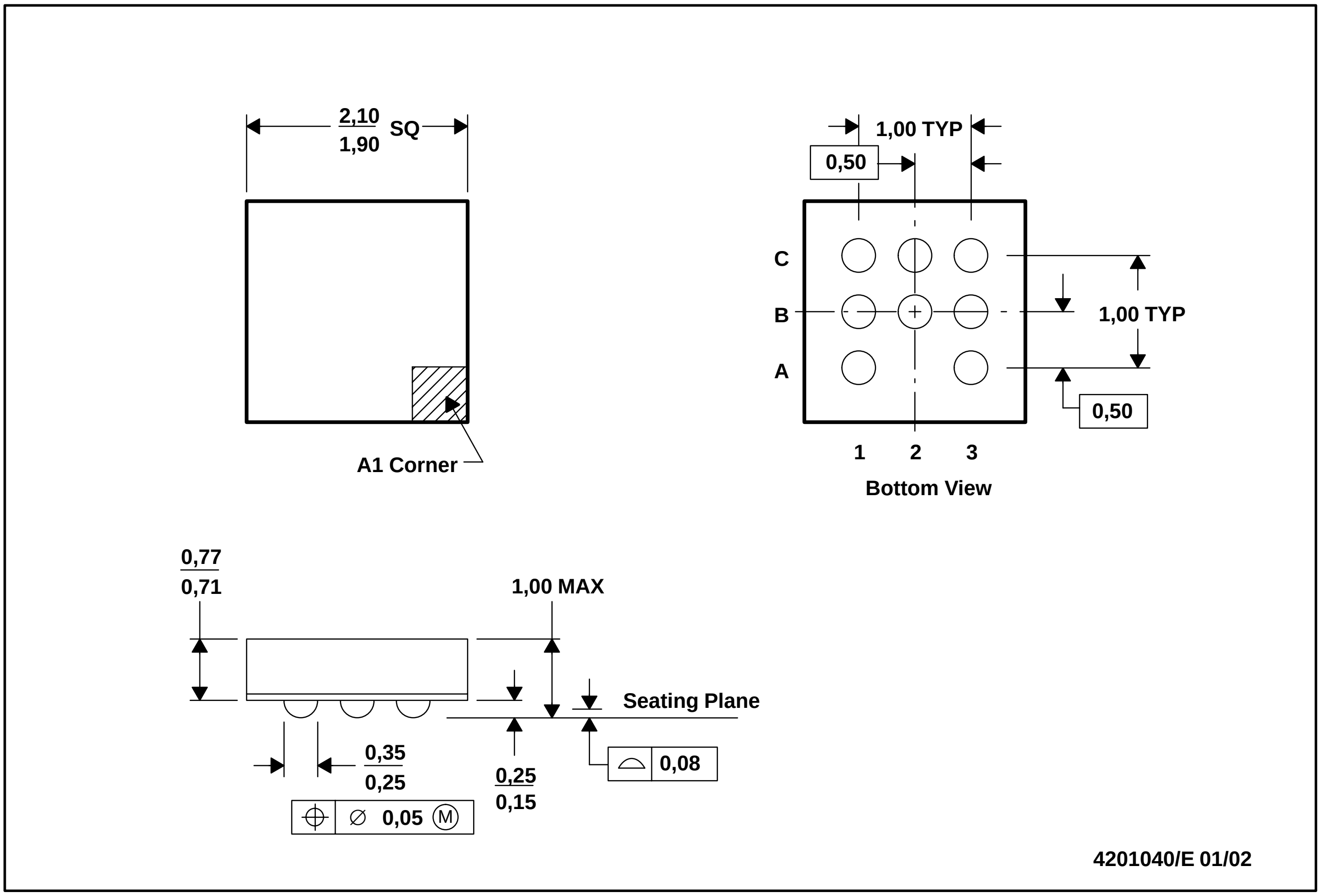
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/C 10/07

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

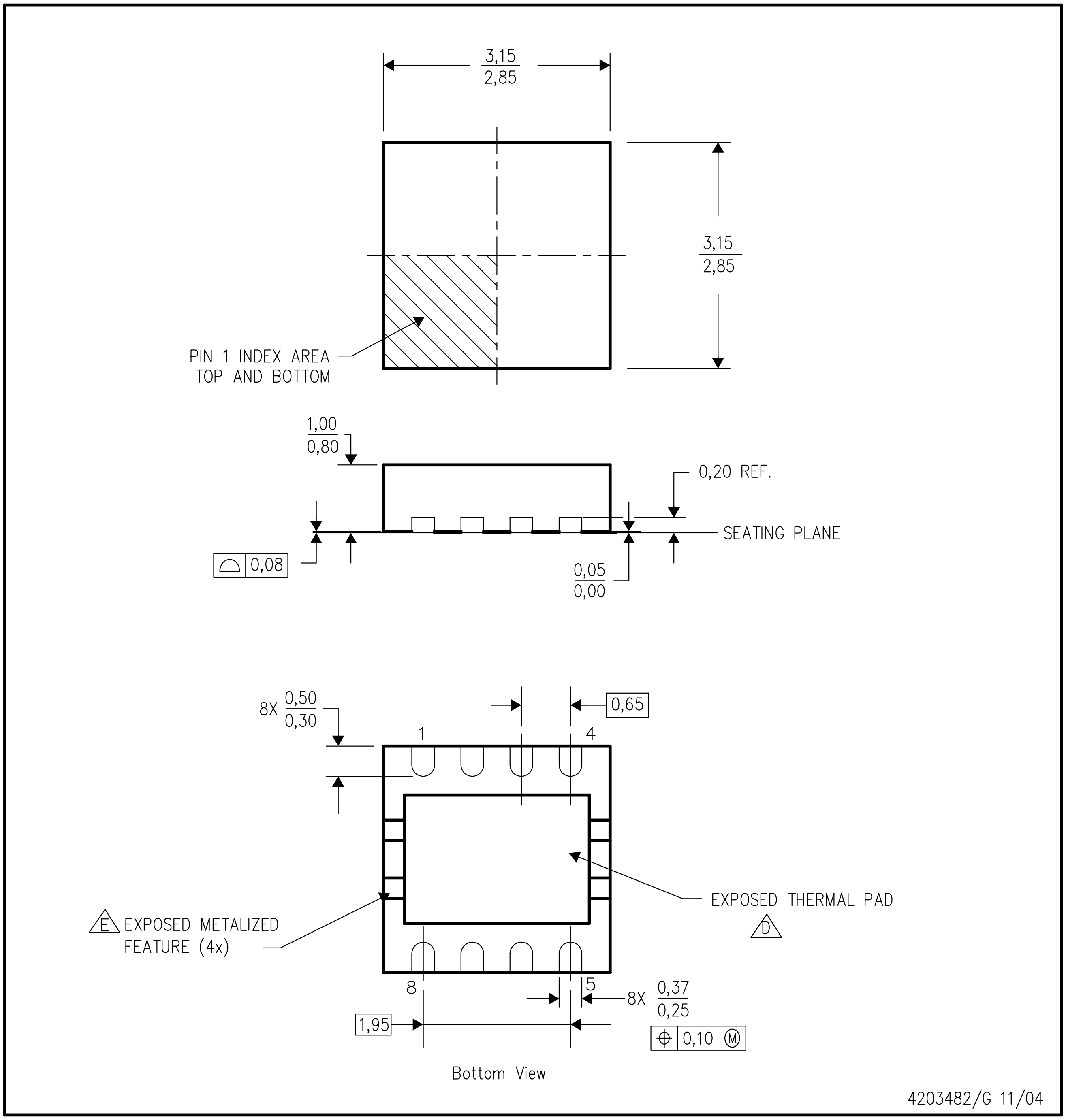
GQV (S-PBGA-N8) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ configuration
D. Falls within JEDEC MO-225

MicroStar Junior is a trademark of Texas Instruments.

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



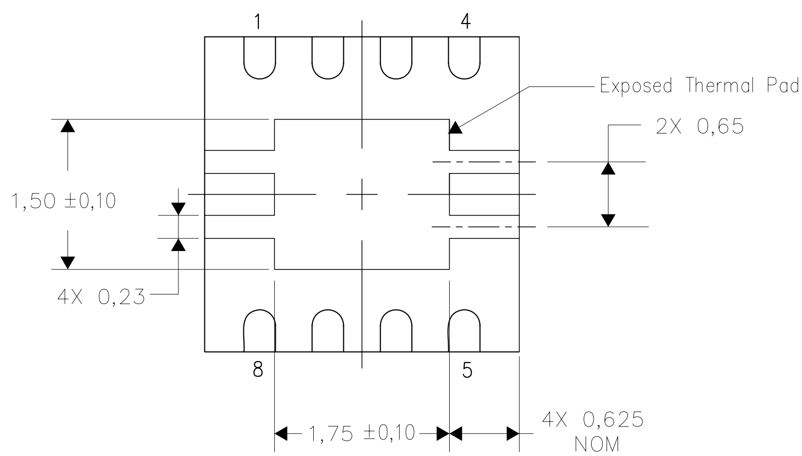
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

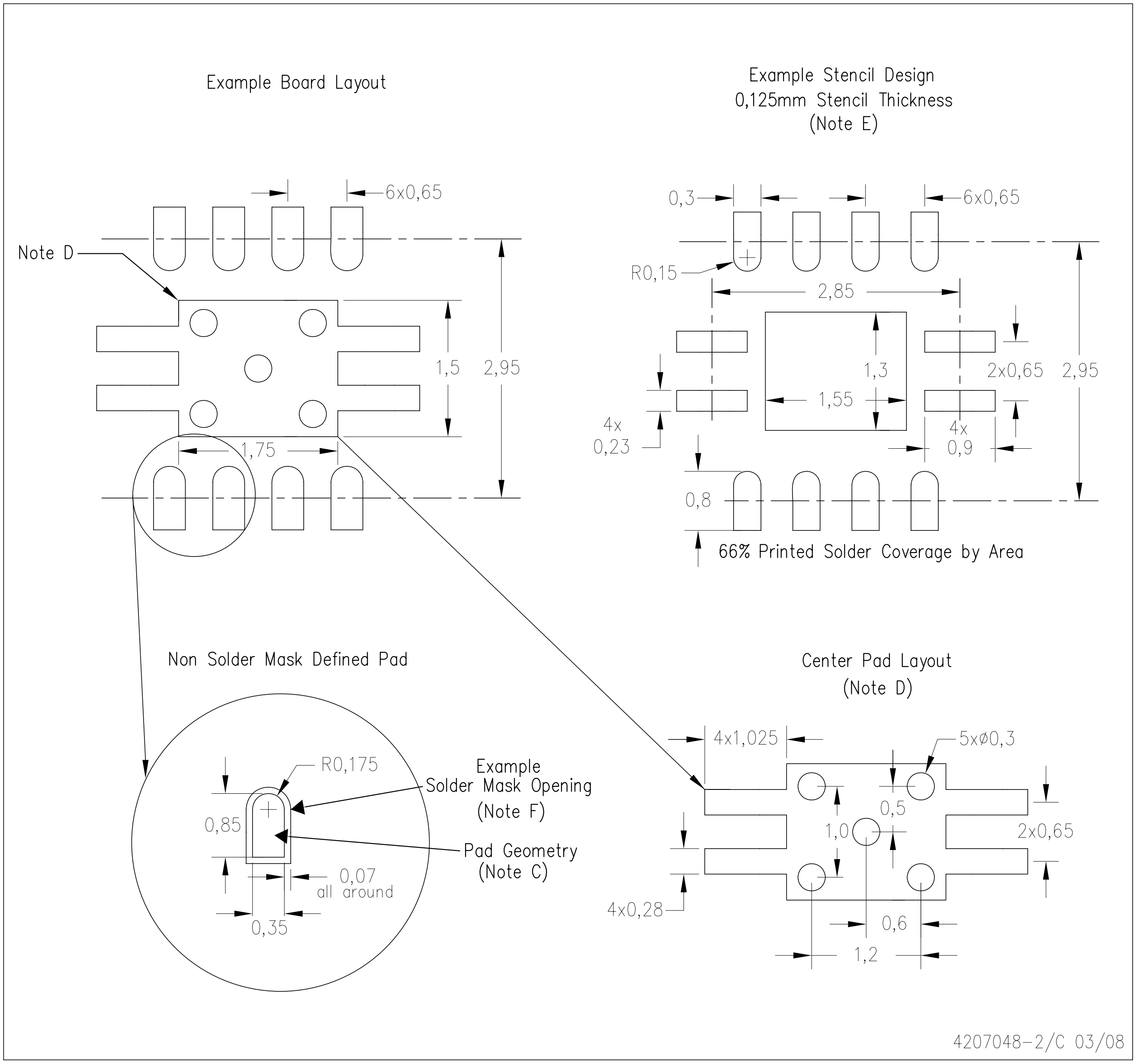


Bottom View

NOTE: All linear dimensions are in millimeters

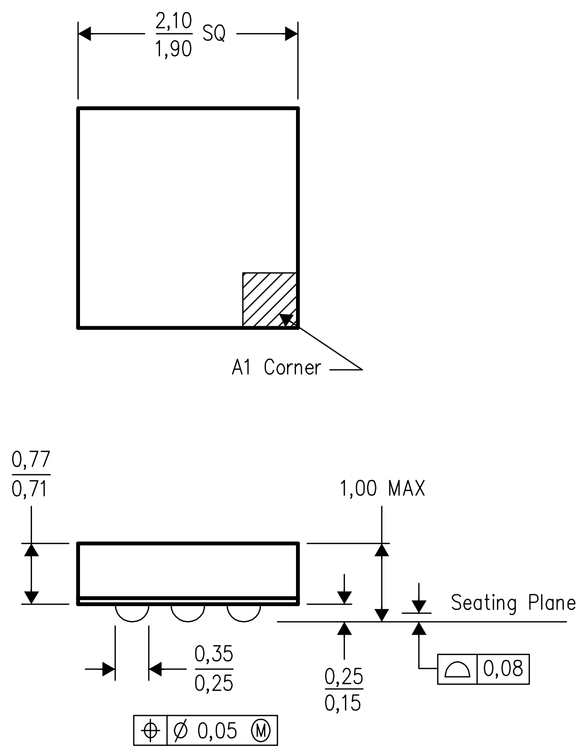
Exposed Thermal Pad Dimensions

DRB (S–VSON–N8)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

ZQV (S–PBGA–N8) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior configuration
- D. Falls within JEDEC MO–225
- E. This package is lead–free.